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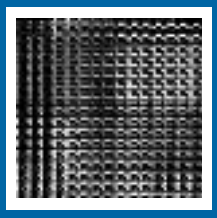

THE OUTLOOK FOR ADVANCED INTERCONNECT METALLIZATION PRECURSORS AND PROCESSES TO THE 70-NM DESIGN RULE

Kline's sixth comprehensive global survey of the market for key semiconductor fabrication materials and processes

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Kline & Company, Inc. has undertaken an in-depth analysis of the trends impacting metallization materials and processes in semiconductor devices. This project complements three recent reports focusing on emerging materials and processing technologies:

- THE OUTLOOK FOR CHEMICAL MECHANICAL PLANARIZATION TECHNOLOGY AND MATERIALS, 2000-2005
- DIELECTRIC MATERIALS IN SEMICONDUCTOR DEVICES TO THE SUB-0.10-MICRON DESIGN RULE, 2001-2006
- THE GLOBAL OUTLOOK FOR RESIST, ETCH, AND CLEANING MATERIALS FOR SUB-0.25-MICRON SEMICONDUCTORS, 2001-2006

Taken together, the three studies provide a core understanding of next-generation materials and processes used in "back-end of the line" (BEOL) semiconductor processing.

THE OUTLOOK FOR ADVANCED INTERCONNECT METALLIZATION PRECURSORS AND PROCESSES TO THE 70-NM DESIGN RULE is designed to help strategic planners involved in materials supply and process tool development for semiconductor and electronic device manufacturing better understand the timing and impact of the inevitable change in semiconductor fabrication practices. It provides information and analysis that will enable strategic planners to effectively anticipate, plan, and respond to the evolution of semiconductor device fabrication processes. Specifically, the report provides subscribers with the following benefits:

- An accurate prediction of the commercial impact and timing of new copper damascene and dielectric technologies on metal precursors in each major semiconductor market segment
- Profiles of metal deposition materials suppliers for possible acquisition/alliance purposes
- An examination of the trends in three major categories of deposition technology: physical vapor deposition (PVD), chemical vapor deposition (CVD), and electrochemical deposition (ECD)

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- Thin film deposition processes
  - Evaporation
  - Physical vapor deposition
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  - Seed depostition
  - Copper electrodeposition
- Environmental issues
- Future deposition trends

4. APPLICATIONS

- Application-specific integrated circuits (ASICs)
- Digital signal processors and microcontrollers
- Microprocessors
- Memory

For each of the above types of semiconductors, the following is provided:

- Description and functions
- Metal deposition operations
- Key end users
- Industry trends

5. METALLIZATION PRECURSOR MATERIALS

- Physical vapor deposition precursor materials
  - Sputtering deposition
  - Ionized sputter deposition
- Chemical vapor deposition precursor materials
  - General CVD precursors
  - MOCVD precursors
  - Precursors and co-reactants for ALD
- Electrochemical and advanced precursor materials
  - Electrodes
  - Electrolytes and additives
  - Electroless deposition
  - Unconventional deposition technologies

For each of the categories listed above, the following is provided:

- Description, including preparation methods
- Grades and prices
- Competing processes
- Current consumption, by end use and region
- Key suppliers
- Outlook, 2001-2006
- Technology trends

6. SUPPLIERS

- Air Products and Chemicals (Schumacher)
- Honeywell Electronic Materials
- Tosoh SMD
- Nikko Materials
- BOC Group
- Praxair
- Other suppliers of consumables

For each significant supplier identified:

- Business form and affiliation
- Estimated sales
- Products
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METALLIZATION ISSUES AND CHALLENGES

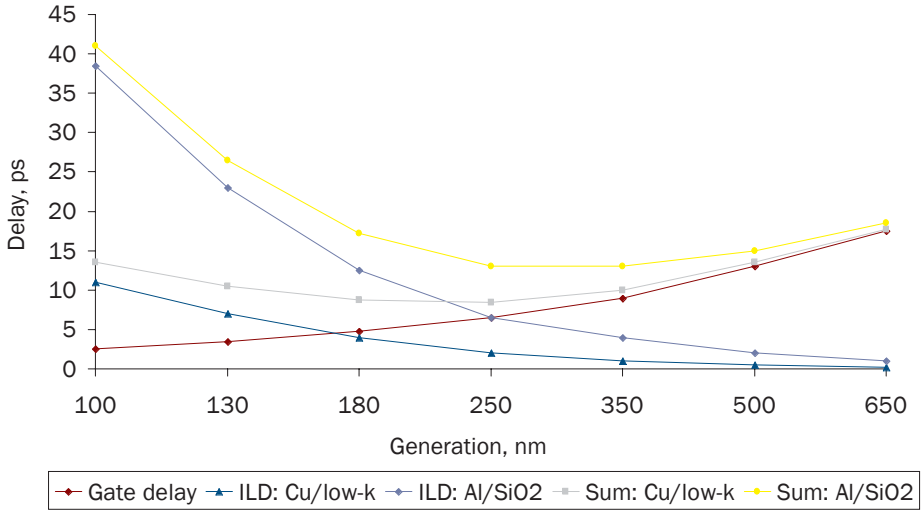
The slowing of signals within semiconductor devices as the scale of integration increases is a function of both metal resistance and capacitance. As metal lines shrink, their cross-sectional area decreases and resistivity rises.

Copper's low resistivity in relation to aluminum helps to overcome some of the rise that is caused by the shrinking geometry. The problem is also alleviated by redesigning the circuit to spread wires out further, or by adding extra layers. Eventually, as design rules lurch down to the 100-nm level, these remedies will not be enough to prevent an increase in the time delay. Fabricators will have to seek cuts in the dielectric constant as well. This is being achieved with low-k dielectrics.

In the current generation of 180-nm circuits, the time delay effect is already being felt. The sum of gate and interconnect delay effects recently bottomed out at the 250-nm level and is now beginning to rise, as shown in Figure 1. Beyond the 180-nm level, the trend accelerates alarmingly if the industry were to continue with conventional aluminum interconnects and SiO_2 insulator. The combination of copper and/or low-k dielectrics can have a dramatic effect on this.

Figure 1

TIME DELAY IN INTEGRATED CIRCUITS BY GENERATIONAL NODE



SOURCE: Bohr, Mark T., "Interconnect Scaling - The Real Limiter to High-Performance ULSI," *Proceedings of the 1995 IEEE Intl. Electron Devices Meeting*, 1995.

Therefore, understanding the evolution of key metallization precursor technologies and metallization deposition processes will be critical to establishing a strong competitive position as the scale of integration continues to increase.

RESEARCH METHODOLOGY

Kline employs a proven, multi-method approach in order to gather, analyze, and confirm the informational inputs that are required to construct a comprehensive report on the global outlook for semiconductor metallization precursors and processes. The components of this multi-method approach include:

- **Field interviews**
  The foundation of information and insight needed to complete this analysis was developed through an extensive series of field interviews with key industry participants across the world, including (1) leading electronic device and semiconductor manufacturers; (2) manufacturers of metallization precursor consumables and deposition equipment; and (3) all pertinent government agencies and trade organizations.
- **Analysis of key insights and industry trends**
  Technological, economic, market, and supply factors were analyzed to assess the current industry structure and to identify key trends that will impact metallization. During this analysis, we utilized knowledge and expertise gained from our previous programs, which covered CMP and dielectric precursors, to assess and realistically predict likely future metallization scenarios as well as to identify potential integration issues and challenges.
- **Proprietary forecasting algorithms**
  Kline has developed a unique forecasting methodology from our previous efforts. The forecasts are based on assessing key industry trends related to the *ITRS Roadmap*, scale of integration and generational standards, device type, and wafer diameter, as well as cost-of-ownership issues.

  Based on this approach, we can calculate wafer starts as well as the number of metal deposits. This proprietary line modeling system projects the markets for consumables and equipment based on device-specific forecasts for interconnection layer counts, design-rule progression, and end-product demand.

SUBSCRIPTION TERMS AND PRIVILEGES

THE OUTLOOK FOR ADVANCED INTERCONNECT METALLIZATION PRECURSORS AND PROCESSES TO THE 70-NM DESIGN RULE is available only by subscription. In order to maximize the value and usefulness to each subscriber, the following privileges and services will be made available:

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- **The option of hard copy or online versions** of the report. Subscribers can elect to receive three hard copies of the report or, alternatively, the online version. The online version includes unlimited access to the report contents for members of the subscribing company via KlineOnline.com, plus one hard copy. Additional hard copies will be made available for a nominal fee.

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QUALIFICATIONS

Kline & Company, Inc. is an international business and management consulting firm offering a broad range of services to the electronics, specialty chemical, and materials industries.

Kline has established a dedicated business and management consulting practice in global electronics and advanced materials that has provided consulting services to organizations active in all sectors of the industry, including electronic systems and devices, batteries, semiconductors, and printed wiring boards, as well as electronic chemicals and materials.

Our headquarters are located in Little Falls, NJ, and we maintain representative offices in:

- Brussels, Belgium
- Melbourne, Australia
- São Paulo, Brazil
- Singapore
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Kline has earned a reputation for delivering high-quality studies and market and technology assessments. We complete approximately 200 proprietary assignments and nearly a dozen multiclient research reports each year.

Over the last ten years, Kline has completed more than 50 projects related to electronic materials and technologies. Many of these assignments have investigated the market opportunities for new technologies with various performance capabilities.

Other projects have evaluated new market opportunities for companies that are considering entering the electronics industry, and Kline has also completed engagements to assist suppliers of electronic raw materials in identifying future material needs.

THE OUTLOOK FOR ADVANCED INTERCONNECT METALLIZATION PRECURSORS AND PROCESSES TO THE 70-NM DESIGN RULE is the latest in a new series of reports on emerging electronic technologies.

In 1999, Kline published a groundbreaking report on the market for slurries, polishing pads, and other consumables used in CMP. This study was titled ***THE OUTLOOK FOR CMP TECHNOLOGY AND MATERIALS, 1998-2003***. This was followed by a complete revision, update, and expansion in 2001, covering the forecast period of 2000 to 2005.

Meanwhile, another landmark study, ***THE GLOBAL OUTLOOK FOR DIELECTRIC MATERIALS IN SEMICONDUCTOR DEVICES, 1999-2004***, was completed in early 2000 and was also updated in 2001 for the forecast period of 2001-2006. A new report on the market for photoresist, etch, and cleaning materials, titled ***THE GLOBAL OUTLOOK FOR RESIST, ETCH, AND CLEANING MATERIALS FOR SUB-0.25-MICRON SEMICONDUCTORS, 2001-2006***, was also released in the spring of 2002.

All reports utilize proprietary line modeling systems that project the markets for consumables and equipment based on device-specific forecasts for interconnection layer counts, design-rule progression, and end-product demand.

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